Design and Comparison of Low-Power Rail-to-Rail with two stage Operational Amplifier Using 180 nm CMOS technology

Anand Kumar Singh, Anuradha , Dr. Vijay Nath

Abstract— In this paper a low power, 1.8V, rail to rail CMOS Op-amp using standard 180nm SCNO technology is proposed and realized. A constant transconductance is ensured for the whole common-mode input range and the class AB output stage provides a full voltage swing. Using this scheme, the Op-amp can obtain a gain bandwidth of 17.3-MHz and a DC gain of 83.67 dB according to the output load. The input transistors operate in weak inversion, which have big gm/Id value, so the power consumption is reduced.

Index Terms— constant g_m, Low power CMOS, 180nm technology, gain margin, phase margin

1 Introduction

With the development of wireless communication, the reconfigurable radio frequency integrated circuit (RFIC) and broadband data conversion circuit facing multi-standard and multimode wireless communication is very important. For the RF front-end transceiver, zero-intermediate frequency scheme is used as there is no image-rejection problem and it consumes less power. A biasing technique using a current switch and a one to one current mirror as used in bipolar technologies [1]. The operational amplifier (Op-amp) we proposed is suppose to be used between the second stage ADC and the down converter in the receiver end, and between DAC and the up-converter in the transmitter end. With the rail-to-rail input and output dynamic range of Op-amp, the ADC and DAC requirements can be lowered and thus system performance can be improved. Also, low power rail-to-rail Op-amp is important for the battery operated devices such as cell phones. To operate the Op-amp at minimum supply voltage has becomes the fundamental job of designing low-power analog and mixed signal systems nowadays. To reach the rail-to-rail amplitude, the input stage and the output stage should be designed respectively.

We can optimize the input stage constant-g_m operation by controlling the total input current. Therefore special biasing schemes have been presented [1-4] to create a rail-to-rail input stage with a nearly constant g, over the full common mode input range.

In fact, as we know, in bipolar process and in MOS weak inversion, the gm is proportional to the current, while in MOS strong inversion it is proportional to the square root of the current. For the high supply voltage, there are some ways to make gm constant. One of the often used ways is 1:3 current mirror. Our main goal is to realize a constant gm input stage and a rail-to-rail output stage for a low-power operational amplifier. This has been achieved by the current-switch transcondutance control circuit in the input stage and the improved class AB in the output one.

2 Design Steps for Two-Stage OP-AMP

In this work, an Op-amp has been designed which exhibits high unity gain frequency for optimize balancing of phase margin, gain, power, and load. A method is proposed to set a higher unity gain frequency of the Op-amp working at a lower supply voltage. This allows the value of each circuit element of the amplifier (i.e. transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required electrical parameters. The g_m variation does not allow optimal frequency compensation of multi-stage op-amps. This effect has been disscussed extensively elsewhere [5]. Here we have chosen a simple differential pair amplifier for input amplifier, common source amplifier (high gain, swing balancing) for output amplifier, a current mirror circuit and a biasing circuit, and connecting PMOS load in input (replacing current source) with a Miller capacitance in series with each other. Designed and simulated circuit Fig. 2 produces DC Gain 54dB and GBW 18.15 MHz. Then we connected same W/L ratio in series with PMOS and NMOS Load. A design steps for two-stage Op-amp in Fig 3 can be constructed as follows.

STEP-1 The aspect ratio for transistor1 and 2 are:

$$S_1 = S_2 = (W/L)_1 \quad (9)$$

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gm1 = GB*Cc
Cc = 0.2 CL
STEP-2 The Vss5 when the transistor is in saturation is:
Vss5(SAT) = Vin(min) – Vss – $\sqrt{}$I5/β1 –VT1
(10)

STEP-3 The aspect ratio of transistor 3 is:
S3 = 2I3 / K3[VDD - Vin(max) - VT(max) + VT(min)]2
(11)

STEP-4 The equation of S5 is
S5= 2 I5/K3 [VDSS5(sat)]2
(12)

STEP-5 The equation of S6
S6 = (gm6/gm4)S4
(13)

STEP-6 The equation of I6
I6 = gm6/2 K6S6
(14)

STEP-7 The equation of S7 is
S7 = (I6/I5)S5
(15)

S9= S10= S11= 1/K'R(VGS-VT)
(16)

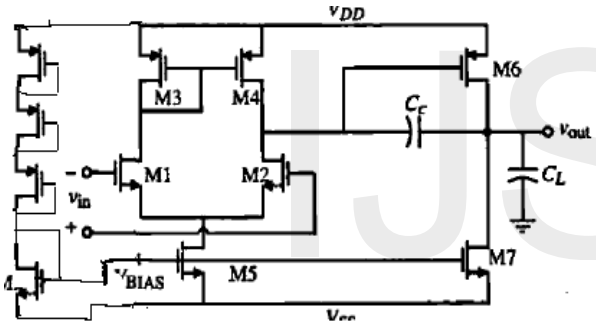

Fig.1 High Frequency Small-Signal Equivalent circuit

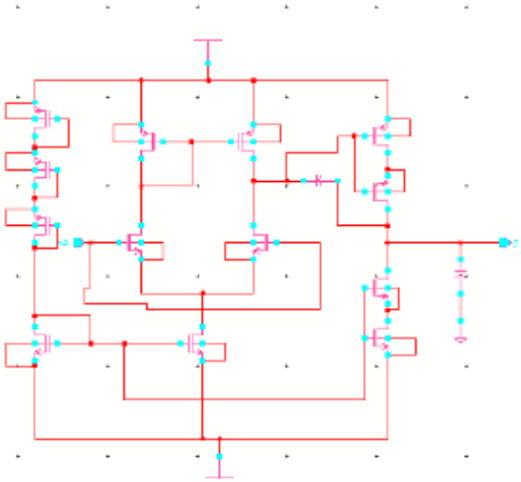

Fig.2 The proposed CMOS Op-amp circuit

By placing two complementary differential pairs in parallel as shown in Fig. 4, it is possible to obtain a rail-to-rail input stage. The NMOS pair is conduction for high input common-mode voltages, in particular

if $V_{SS}+ V_{gsn}+ V\text{dsat} < V\text{common}$
(17)

While the pMOS pair is in conduction for low input common-mode voltages
$V\text{common} < V_{DD} - V\text{dsat} - V_{sgp}$
(18)

When both pair are in parallel, the input dynamic range can be
$V_{ss} < V_{Common} < V_{DD}$
(19)

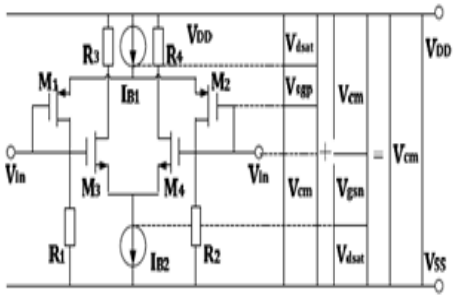

Fig 3. The input range of complementary differential pair

To ensure that the proposed circuit is rail-to-rail, the minimum supply voltage should be

$V_{sup,min}= Vsg,p + V_{gsn} + V_{d,sat,n} + V_{d,sat,p}$ (20)

However, a main shortcoming of a rail-to-rail structure is that its total transconductance will change. That is, when the input voltage can make both pairs on, its total transconductance will be twice of that when only either pair is on. This will bring to the change of the loop gain and thus cause distortion. The weak-inversion" architectures [6], [7] shows how to get constant transconductance. As the transistors in the proposed circuit work in weak inversion, their transconductance are proportional to the currents in them

$g_{mi\ weak} = I_p/2n_pV_T+I_n/2n_nV_T$ (21)

Where, I_p and I_n are the current in the PMOS and NMOS pair, n_p and n_n are slope factors of the weak inversions. V_T is the thermal voltage. So, to make g_m constant, we can tune the current within the input range. As can be seen from Equation (22) and Fig. 2, we set V_{bias} voltage to be 0.9 V. When the input voltage is low enough, PMOS differential pair M1 and M2 are on while NMOS differential pair M3 and M4 are off. Then, I_{b1} will come through M1 and M2, I_{b2} will come through M15 and M16, and so the total g_m will be

$g_m = g_{mp} = I_p/2n_pV_T$ (22)

When the input voltage is high enough, NMOS transistorsM3 and M4 are on while PMOS transistors M1 and M2 are off. Ib1 will pass through M13 and M14 while Ib2 though M3 andM4, thus the total gm will be
gm =gmn = In/2nnVT (23)

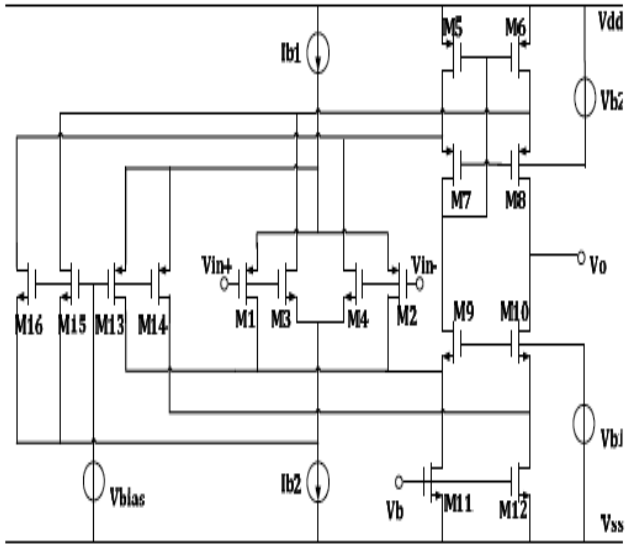

Fig.4. Current switch transconductance control circuit

When the input voltage is in the middle range, both pairs are on, the current switch M13, M14, M15, M16 will take away some of the current from Ib1 and Ib2, thus the total gm will be

$$gm=gmp+gmn=Ip/2npVT+ In/2nnVT \quad (24)$$

Suppose the input voltage is 0.9 V, here M1~M4 will take 1/4 of the tail current, the expression will be

$$gm=Ip/4npVT+In/4nnVT \quad (25)$$

To have gm constant, we should modify transistor size to Make

$$Ip/np=In/nn \quad (26)$$

Here the input stage delivers a constant output current to the summing circuit, which consist a high-swing current mirror (M5-M8) and common-gate stage (M9,M10). Gain can be improved by raising the tail current, however, to make sure input transistors are in weak inversion, the width and length of input transistors should be improved which at the same time can lower the offset of the circuit Output stage.

In this work, output stage takes the improved feed-forward class AB circuit. For this circuit as shown in Fig. 3, M27 and M28 are the output part. M19 and M20 form a class AB control circuit. Points A and B have a small DC voltage, which can make sure that output transistors will not both be off thus to avoid cross-over distortion.

$$Vgs19+Vgs27=Vgs22 + Vgs23 \quad (27)$$

$$Vgs20+Vgs28=Vgs25 + Vgs26 \quad (28)$$

Let M19 and M22, M20 and M25 have the same size, then-Vgs27 = Vgs23, Vgs28 = Vgs26. The quiescent current can thus be expressed as

$$Iq=W/L27/W/L23I21 \quad (29)$$

Here we suppose the currents in M21 and M24 are the same, and the following equation is satisfied

$$(W/L)27/(W/L)28=(W/L)23/(W/L)26= (W/L)22/(W/L)25 =(W/L)19/(W/L)20 \quad (30)$$

To make the quiescent current stable, M29 and M30 are added as floating current source, so as to bias the class AB control circuit. Here M29 and M30 has two parts to play, one is to compensate the affect of voltage source, as they are the same structure of M19 and M20. In this way, PSRR of the circuit can be improved. The second is to make the quiescent current stable, less affected by the common mode input voltage. Different from the techniques handling the dc tail current, a method based on processing signal current has been proposed [8]. A novel implementation that employs a diverting transistor of the same size as that of the driving transistor has been reported [9]. All these implementations require more chip area and power consumption compared with the conventional input stage. Furthermore, these techniques often have degraded CMRR [10], [11].

The whole circuit can be seen in Fig. 4, the cascaded Miller frequency compensation method was used. Compared to the classical Miller compensation, this method shifts the non-dominant pole to higher frequency[12]-[14].

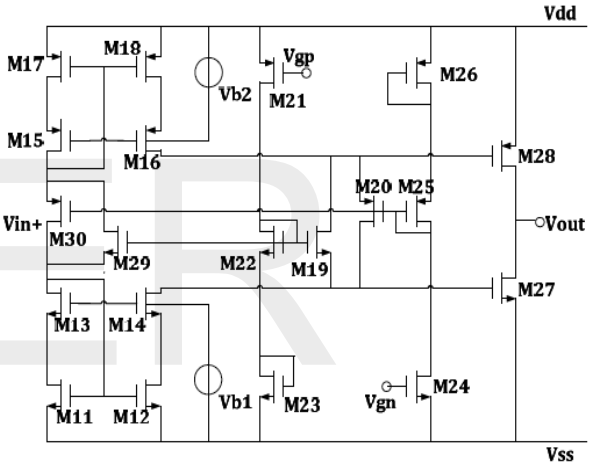

Fig. 5 The improved output structure with floating current source

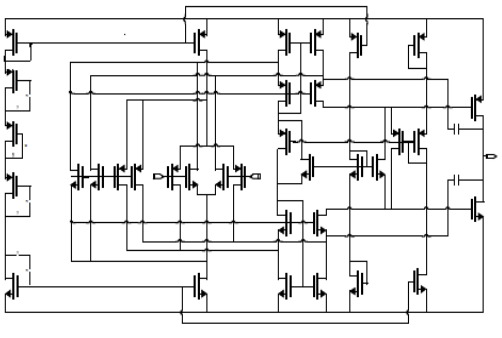

Fig. 6 The proposed Op-amp circuit diagram

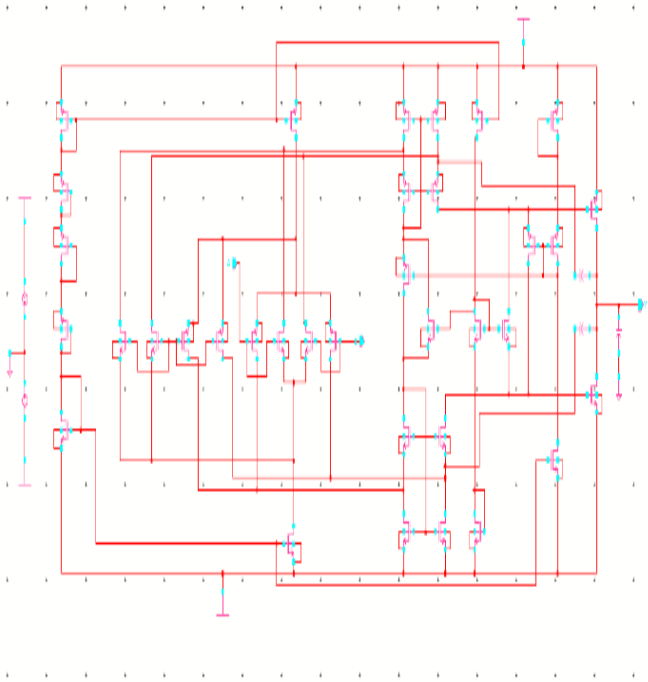

Fig. 6 The proposed Op-amp circuit on test bench

3 SIMULATION RESULTS

Based on the proposed circuit in Fig.2 and Fig.6 Op-amp has been designed 180nm CMOS technology. The Op-amp is currently being fabricated in SCNO and their simulation results are presented. The electrical specifications of CMOS Op-amp and process parameters for 180 nm CMOS technology are tabulated in the Table I and Table II respectively. Fig. 7 represents the frequency response of the Op-amp for different Vi,cm values. The achieved DC gain (Av0), gain bandwidth product (GBW) and phase margin (PM) are 153.3dB, 17.9 and 83.67 respectively.

Table I
Electrical specification of CMOS Op-amp

$\mu C_{ox}/2$: NMOS (A/V^2)	173.9
$\mu C_{ox}/2$: PMOS (A/V^2)	35.0
$V_{th,p(min)}$ (volt)	0.37
$V_{th,n(max)}$(volt) NMOS	0.50
ICMR(Volt)	1.3
V_{dd}(volt)	1.8

3.1 AC RESPONSE

Through AC response we can simulate the schematic to find out the bode plot and phase plot. In Fig 7, a bode plot and phase plot for 1.8 V, 27° C and CL = 5 pf is shown. As can be seen, the open loop gain is 83.67 dB, and a phase margin is 26.69°. The unity gain bandwidth is 17.15 MHz and bandwidth is 2.693 KHz.

Table II
Process Parameters of 180 nm CMOS Technology

Load capacitance: CL (pF)	10
Miller compensation capacitances: CC (pF)	3
Supply voltage	+1.8 V

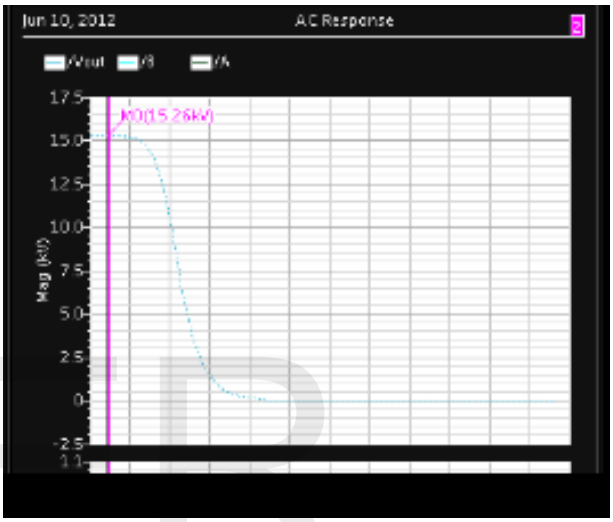

Fig 7.Frequency Response Plot with C_L=5pf

3.2 TRANSIENT STEP RESPONSE

In Fig 9, a step from ground to V_{DD} is applied at the input with unity feedback configuration. The slew rate of Op-amp is 11.22 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse.

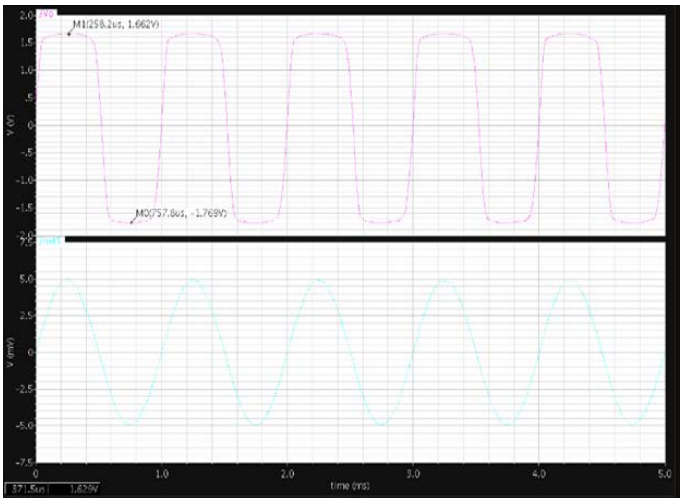

Fig 8.Transient Pulse Response of Op-amp

3.3 GAIN AND PHASE

Gain and phase Fig-9 and Fig-10 shows DC gain and Phase .its represent DC gain is 83.67db and phase 136 deg at vdd=1.8 and SCNO 180nm tech.

Fig9 .Dc Gain of Op-amp

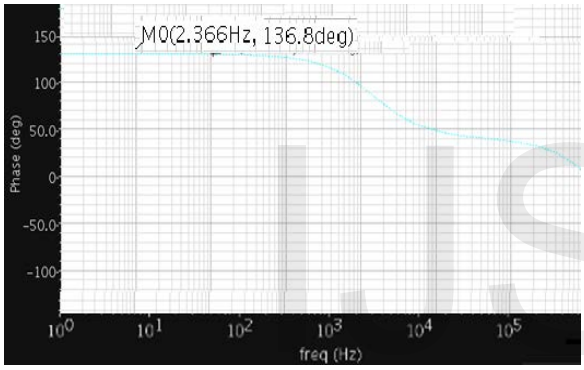

Fig. 10 Phase of Op-amp

3.4 PHASE AND GAIN MARGIN

Phase and Gain margin-fig 11 shows that phase margin is 153.3 deg and gain margin is 68.36 db after simulation in applied voltage 1.8 and gain 83.67db and phase 136.6deg.

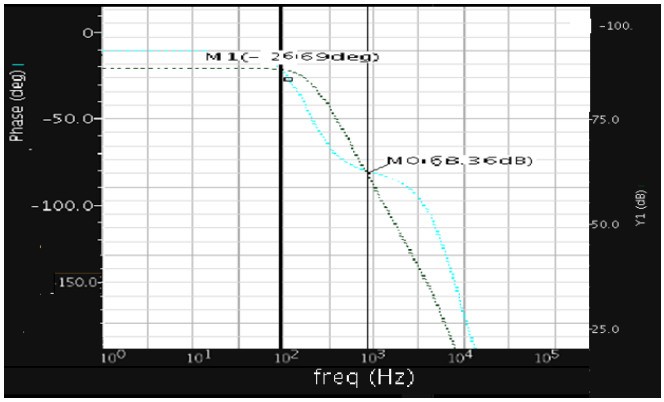

Fig. 11 phase and gain margin of Op-amp

Table III.
Comparison of Simulation Results of two stage and rail to rail class AB control CMOS Op-amp (180nm Technology)

Specifications	Simulation results	Simulation results
DC gain (dB)	62.05	83.67
GB (MHz)	18.9	17.9
Phase margin	166.31	153.3
Gain margin	28.36	68.6
CMRR (dB)	159.5	178.8
ICMR (V)	1.3	0.9
Slew rate (V/μS)	11.23	11.20
Power dissipation(μW)	121.4	99.4
I_{D5}(μA)	33.78	11.8
I_{DL}(μA)	140.4	60.1
Load capacitance (pf)	10	5

4 CONCLUSION

The proposed Op-amp is simulated at 180 nm using cadence virtuous and the performance is measured. With this proposed structure excellent result of dc gain, phase, slew rate, phase margin and gain margin have been achieved. The dc gain and GBW graphs show increase DC gain decrease GBW frequency. The Fig. 8 shows transient response, Fig. 9 DC gain, Fig 10 shows phase, gain margin and Fig11 shows phase margin. In table 3 we simulate the proposed Op-amp at 180 nm and measure the performance.

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